Description

SWITCHING-TYPE POWER CONVERTER

BACKGROUND OF INVENTION

[0001]   This invention relates to switching-type power converters and in particular to the reduction of power loss and heat dissipation of such converters over a wide load range of operation.

[0002]   Power converters can be divided into linear type and switching type. The switching converter has the great advantages of light weight, small size and greater efficiency compared with the linear converter.

[0003]   A typical dc-dc switching converter circuit such as the one shown in Fig. 1 receives input power from input terminals 24, 26 and produces a switching waveform across the primary winding 28 of transformer 32. The electric power entering primary winding 28 is coupled to secondary winding 30 which feeds the power to a rectifying circuit which in turn outputs converted power to load 38.

[0004]   The basic forward converter topology shown in Fig. 1 is probably the most widely used topology for powers under

300 W. Input capacitor 20 compensates for the inductance of the cable supplying the input dc power at nodes 24, 26.

[0005] When switch 40 is turned on by pulse generator 34, the dot end of secondary winding 30 of transformer 32 goes positive with respect to its no-dot end. Diode 42 is for-ward-biased, and current flows out to lowpass filter 44, 48. The lowpass filter averages the output waveform and diode 46 works like a free-wheeling diode. When switch 40 turns off, the magnetizing energy stored in trans-former 32 is reset by reset circuit 36.

[0006] A large portion of the power loss and heat dissipation is due to the switching loss of switch 40 (e.g. FET). This switching loss results from the overlapping of non-zero voltage and current waveforms during the switching tran-sient.

[0007] In order to reduce the switching loss, the switching tran-sient time and switching frequency should be reduced. But these techniques have some drawbacks. Using a low switching frequency will lead to larger magnetic compo-nents such as a larger transformer and a larger inductor. And when the switching transient becomes very fast, the current slope (di/dt) and voltage slope (dv/dt) will become very large and may cause serious noise problems.

[0008] One possible way of reducing the switching loss is the zero-voltage switching method. In practice, the zero-voltage switching method is not completely satisfactory in commercial power conversion products. In order to perform the zero-voltage switching function, a special IC or many more components are usually required, thereby increasing the size and production cost of the power converter. In practice, in order to design a resonant path, some bulky passive components are used (such as a large choke) that increase the size and conduction loss of the converter.

[0009] Because of the complexity of the resonant circuit and the control loop, tedious calculations and computer simulations are usually needed. This complicates product design and production. For example, a phase-modulated full-bridge topology can be designed to achieve zero-voltage switching only for a narrow band of output loading. When operated outside of its narrow loading range, it enters the hard-switching mode that greatly increases the heat loss. In general, designing a reliable zero-voltage switching circuit that can cover a wide loading range is very difficult. Thus, there is a continuing need to improve the zero-voltage switching method.

Brief Description of Drawings

[0010] FIG. 1 is a schematic of a typical switching-type power supply circuit currently used in dc-dc conversion circuits.

[0011] FIG. 2 is a simplified diagram showing an example of connections using a fixed-frequency driver and a resonant capacitor across the switch.

[0012] FIG. 3 is a simplified diagram showing an example of connections using a fixed-frequency driver and a resonant capacitor across the primary winding of a transformer.

[0013] FIG. 4 is a schematic diagram showing the use of a pulse width extension tracking (PWET) circuit to track the zero-voltage switching point.

[0014] FIG. 5 shows an embodiment of the invention using diodes and a transistor to perform the OR gate function in the PWET circuit.

[0015] FIG. 6 shows the schematic waveforms for the PWET circuit.

[0016] FIG. 7 is a simplified diagram showing an example of connections using a variable-frequency PWET circuit.

[0017] FIG. 8 is a simplified diagram showing the use of a full bridge circuit in obtaining a regulated root-mean-square ac output.

[0018] FIG. 9 shows the voltage across the switch of the con-

verter for no-loading current.

[0019] FIG. 10 shows the voltage across the switch of the converter for full-loading current.

[0020] FIG. 11 shows the measured gate voltage and the voltage across the switch for the converter of FIG. 5.

[0021] FIG. 12 is a simplified diagram showing the use of a loading-independent zero-voltage switching (LIZVS) circuit and current ripple cancellation (CRC) circuit.

[0022] FIG. 13 shows the output stage connecting to a full-bridge dc-ac circuit.

[0023] FIG. 14 shows the efficiency of a 75-W inverter based on the topology of FIG. 1.

[0024] FIG. 15 shows the efficiency of a 75-W inverter based on the topology of FIG. 8.

DETAILED DESCRIPTION

[0025] The preferred embodiment of the invention consists of (1) loading-independent zero-voltage switching (LIZVS) circuit, (2) pulse width extension tracking (PWET) circuit, and (3) current ripple cancellation (CRC) circuit.

[0026] The LIZVS circuit is shown in Fig. 2. Zero-voltage switching is used to reduce the switching loss. The resonant elements are primary winding 28 of transformer 32 and capacitor 22. The capacitor can be connected alternatively

across transformer primary winding 28 as shown in Fig. 3.

[0027] In order to make the resonant characteristic independent of the loading current, current flow through transformer secondary winding 31 is blocked by the reverse biasing of diode 42 when the primary winding 28 and capacitor 22 resonate. Consequently, there is no secondary current to affect the inductance of primary winding 28.

[0028] Input nodes 24 and 26 (reference) connect to input capacitor 20. Pulse generator 50 drives switch 40. When switch 40 turns on, current flows through primary winding 28 of transformer 32 and bypasses capacitor 22, thereby coupling power to secondary winding 30 of transformer 32. Diode 42 and capacitor 54 convert the ac signal induced in secondary winding 30 to a dc output. The power is delivered directly to load 52.

[0029] When switch 40 turns off, the flowing input current charges capacitor 22. The voltage across switch 40 rises slowly compared with the current drop through the switch. Hence, the turn-off loss is greatly reduced. The voltage across switch 40 starts to resonant with the frequency determined by the values of the inductance of primary winding 28 and the capacitance of capacitor 22. During resonance, diode 42 is reverse biased so that there

is no current passing through secondary winding 30. Hence, the inductance of primary winding 28 remains constant during resonance.

[0030] When the voltage across switch 40 decreases and reaches zero, switch 40 is turned on again by a positive drive voltage on gate 23. Since the voltage across switch 40 is zero, the turn on switching loss is theoretically zero. After switch 40 is turned on, the resonance ends because switch 40 short-circuits the capacitor. And secondary winding 30 output current begins to flow again. In this manner, the switching loss of switch 40 is greatly reduced.

[0031] Pulse generator 50 may include a value-entry device which allows a user to specify the switch-off repetition rate or alternatively the switch-on time duration.

[0032] Fig. 9 shows the voltage across switch 40 for no-loading current during resonance of primary winding 28 and capacitor 22. Fig. 10 shows the voltage across switch 40 for full-loading current during resonance. Figs. 9 and 10 illustrate that the amplitude and frequency of the voltage across switch 40 during resonance is independent of the loading current.

[0033] The switching transformer 32 plays two roles in this in-

vention. One is to couple the power from input to output and the other is to act as an inductor. When diode 42 is forward biased, transformer 32 couples the power. Transformer 32 becomes an inductor when diode 42 is reverse biased. Hence, no additional bulky inductor is needed to generate a resonant waveform. Moreover, the voltage across and current through capacitor 22 have sine-wave patterns that reduce the electromagnetic interference.

[0034] According to this invention, the resonant characteristic is independent of the loading current and has the following merits: (1) The switch 40 is subject to zero-voltage switching over a very wide loading range; (2) Very flexible combinations of circuits: e.g. control stage 78 and output stage 56; (3) Fixed switching frequency can be used; (4) Fixed switching duty cycle can be used; (5) No need to add a large inductor for resonance; (6) Output inductor is not necessary; (7) No snubber circuit is needed; (8) Low EMI.

[0035] Fig. 8 shows an output stage 130 using a full-bridge dc-ac topology. The dc-voltage available from capacitor 118 is applied to the bridge consisting of MOSFET switches 106, 108, 110, and 112. Controller 114 alternately turns on switch pair 106, 112 and switch pair 108, 110, thereby

causing current to flow periodically through load 52 in alternate directions. This arrangement can provide a regulated root-mean-square (rms) ac output by utilizing a pulse width modulation (PWM) controller. PWM controller 114 regulates the output rms voltage by controlling the duty cycle of switches 106, 108, 110, and 112.

[0036] Tests of two power inverters illustrate the high-efficiency of this invention. The first inverter uses the conventional forward converter topology (similar to Fig. 1). Its rated power is 75 W and the result is shown in Fig. 14. The second inverter uses the circuit of Fig. 8 which embodies the principles of this invention. Its rated power is also 75 W and the result is shown in Fig. 15. Figs. 14 and 15 illustrate the improvement in efficiency that can be realized with the present invention.

[0037] Switch 40 of Figs. 3 and 4 can easily be controlled by a fixed-frequency signal generated, for example, by a simple self-oscillating pulse generator. The pulse-width extension tracking (PWET) circuit, a zero-voltage tracking circuit, provides a more precise control signal or even a variable-frequency control signal.

[0038] FIG. 4 shows the PWET circuit 78 used to control the LIZVS circuit discussed above. It senses the voltage across the

switch 40. When the switch turns off, the voltage across capacitor 22 first increases and then decreases to zero. When the voltage reaches zero, the PWET circuit lets the switch turn on again. The switching frequency is determined by the setting of the pulse repetition rate of pulse generator 50 as part of the design process or by the user entering a value via the value-entry port.

[0039] Pulse generator 50 operates at a specified frequency and a narrow pulse width. The pulse signal is supplied to pulse shaper 60 and OR gate 62. The output of OR gate 62 drives switch 40. Comparator 68 senses the voltage across switch 40. When the voltage goes to zero, the comparator output goes high. The output of comparator 68 is fed into OR gate 62. OR gate 62 output is high if either of its inputs is high. As a consequence, the pulse out of OR gate 62 corresponds to the pulse of pulse generator 50 extended in width into the past by overlap with the pulse from comparator 68.

[0040] In order to prevent circuit latch-up, pulse shaper 60 provides a signal to comparator 68 to turn it off when pulse generator 50 outputs a high signal. The trailing edge of the pulse produced by pulse shaper 60 prevents comparator 68 from reacting to the initial zero voltage across

switch 40 when the pulse from pulse generator 50 ends and switch 40 is turned off.

[0041] Fig. 5 shows a functionally-equivalent circuit substituted for OR gate 62 in Fig. 4. When either input to diodes 51 and 53 goes high, voltage node 23 also goes high causing switch 40 to turn on. If the inputs to both diodes are zeros, transistor 57 turns on, voltage node 23 discharges to ground through the transistor, and switch 40 turns off.

[0042] Fig. 6 shows the waveforms of the PWET circuit. It illustrates that the pulse output from pulse generator 50 seems extended into the past to the zero-voltage switching point.

[0043] Fig. 11 shows the measured voltage across switch 40 (upper trace) and the voltage at node 23 (lower trace) for the circuit configuration of Fig. 5. In order to provide a better understanding, a slightly lower voltage is used to represent the pulse coming from pulse generator 50.

[0044] In summary: (1) Switch 40 is closed by the high output of comparator 68; (2) Switch 40 is opened by the low output of pulse generator 50; (3) The pulse output by pulse shaper 60 terminates the high output of the comparator; (4)If there were no pulse shaper 60, the circuit would latch up as follows: (a) comparator 68 going high followed by

(b) OR gate 62 going high followed by (c) switch 40 closing resulting in (d) voltage across switch 40 being zero resulting in (e) comparator 68 going high and remaining high.

[0045] The PWET circuit 78 is a particular embodiment of what might be called more generally a "controller". A controller, in the context of the present invention, provides the means for turning switch 40 on and off. The simplest form of a controller is one which periodically supplies a switch-off voltage having a duration equal to one-half the reciprocal of the resonant frequency of primary winding 28 and capacitor 22. When the controller is not supplying a switch-off voltage, it supplies a switch-on voltage. Pulse generator 50 is a particular embodiment of this simplest form of controller.

[0046] In the more sophisticated versions of a controller, the voltage across switch 40 is supplied to the controller and the controller supplied voltage changess from the switch-off voltage to the switch-on voltage by examining the voltage across switch 40 (see Fig. 11). The appropriate time to switch from the switch-off voltage to the switch-on voltage is when the switch-40 voltage goes to zero.

[0047] A zero switch-40 voltage is easily determined with a com-

parator which compares the switch-40 voltage with zero and produces a switch-on signal when the switch-40 voltage is substantially equal to a zero reference level. A switch-on signal from the comparator is not sufficient in itself, however, to indicate when the change from the switch-off voltage to the switch-on voltage should occur since the comparator output signal will be produced when the switch-on voltage is being supplied by the controller to switch 40. Thus, some means must be provided for either ignoring the comparator output signal or deactivating the comparator during the time period when the controller is transitioning from the switch-on voltage to the switch-off voltage.

[0048] The PWET circuit 78 deactivates the comparator during the time period when the controller is transitioning from the switch-on voltage to the switch-off voltage. Another approach would be to block the switch-on signal from the comparator for a short time interval after the controller switches from the switch-on voltage to the switch-off voltage. Still another approach would be to require the switch-40 voltage to be substantially different from zero prior to allowing the comparator to respond to a zero switch-40 voltage. For example, the reference level for

the comparator could be set at a voltage substantially different from zero when the switch is turned off. When the comparator determines that the switch-40 voltage matches the reference level, then the reference level for the comparator is reset to zero.

[0049] Fig. 7 shows an embodiment of the invention wherein the LIZVS converter together with a PWET circuit are used to regulate the output voltage. The waveform issuing from secondary winding 30 and diode 42 is passed through lowpass filter 90, 54 for averaging. Free-wheeling diode 92 keeps the current flowing when diode 42 is reverse biased. The PWET circuit senses the averaged dc output voltage via connection 101. Pulse generator 50 obtains an error signal by differencing voltage 101 and a desired value established within pulse generator 50 by design or entered by the user via the value-entry port. Pulse generator 50 adjusts the switch-on time of switch 40 to obtain a zero error signal thereby maintaining the output voltage at a value equal to the desired value maintained within pulse generator 50.

[0050] With this configuration the output voltage is a function of duty cycle. Because the switch-off time must be maintained equal to one-half the reciprocal of the resonant

frequency, the switch-on time is the only quantity available for adjustment. Hence, voltage 101 is fed to pulse generator 50 to adjust the switch-on time to regulate the output.

[0051] The capacitors used in the power converteral also entail power loss, especially in high-current operations. When current flows in and out of a capacitor at a high frequency, the power loss will be significant. The CRC configuration can reduce the heat dissipation in the capacitors.

[0052] The CRC configuration is the combination of at least two LIZVS circuits with each LIZVS circuit working with a switch-on duty cycle no higher than 1/N where N is the number of LIZVS circuits in the combination. Only one LIZVS circuit is in a switch-on state at any one time.

[0053] Fig. 12 shows a CRC configuration involving two LIZVS circuits. Input power is supplied at nodes 162, 164. Capacitor 154 is the input capacitor which compensates for the inductance of the cable supplying power to nodes 162, 164. Capacitors 150, 158 and primary windings 140, 144 of transformers 136, 138 constitute the resonant circuits associated with the two LIZVS circuits. Pulse generator 148 alternately supplies a switch-on voltage to primary

switches 152, 156. The switch-on times of primary switches 152, 156 do not overlap. The power outputs from transformers 136, 138 can be treated as two separate and distinct voltage sources and can be connected either in parallel or in series. The two LIZVS circuits alternately supply current through secondary windings 132, 146 and diodes 132, 134 to capacitor 82 and load 52.

[0054] Fig. 13 shows a CRC configuration for a dc-ac power converter utilizing the full-bridge dc-ac circuit of Fig. 8. The CRC configuration is very suitable for dc-ac power inversion because the input voltage is usually low and the input current is usually large. When the CRC circuit is used, the heat dissipation of input capacitor 154 is greatly reduced.